

Inditional toomunications, LMIS and other millimeter wave applications, the TR332001 is an ab used in conjunction with other driver or power amplifiers to achieve the required total power output. Features 19 dB small signal gain (typ.) 22 dBm saturated power out (typ.) 21 cmit contains individual source vias 22 hips Size 4.28 mm x 3.19 mm x 50 µm Absolute Ratings 	Description	The iTR39200 is a high (officion		vor a	molifier	designed	for use in point	t to p	oint radi	io no	nint to
 9.3 (2 dbm saturated power of (yp.) Circuit contains individual source vias: Circuit contains individual source vias: Circuit contains individual source vias: Chip Size 4.28 mm x 3.19 mm x 50 µm	·	The iTR39200 is a high efficiency power amplifier designed for use in point to point radio, point to multi-point communications, LMDS and other millimeter wave applications. The iTR39200 is a 3-stage GaAs MMIC amplifier utilizing an advanced 0.15µm gate length Power PHEMT process and can be used in conjunction with other driver or power amplifiers to achieve the required total power output.										
Ratings $Parameter$ SymbolValueUnitPositive DC Voltage (+5 V Typical) Negative DC Voltage (+5 V Typical) Negative DC Current Simultaneous (V ₀ - V ₀) Positive DC Current Storage Temperature Range Thermal Resistance (Channel to Backside) V_{00} $+ 6$ Volts Volts Volts 0 Electrical Characteristics (At 25°C) 50 Ω system, V ₀ =+5 V, Quiescomt current (t ₀₀) = 1600 mA Parameter Min 	Features	 32 dBm saturated power out (typ.) Circuit contains individual source vias 										
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Negative DC Voltage Simultaneous (V0, -V0,) Positive DC Current RF Input Power (from 50 Ω source) Operating Base plate Temperature Storage Temperature Range Thermal Resistance (Channel to Backside) V_0^2 V_{00s} H_8 I_5 <b< th=""><th>Ratings</th><th></th><th></th><th>(</th><th>T :</th><th></th><th>-</th><th></th><th></th><th></th><th></th><th></th></b<>	Ratings			(T :		-					
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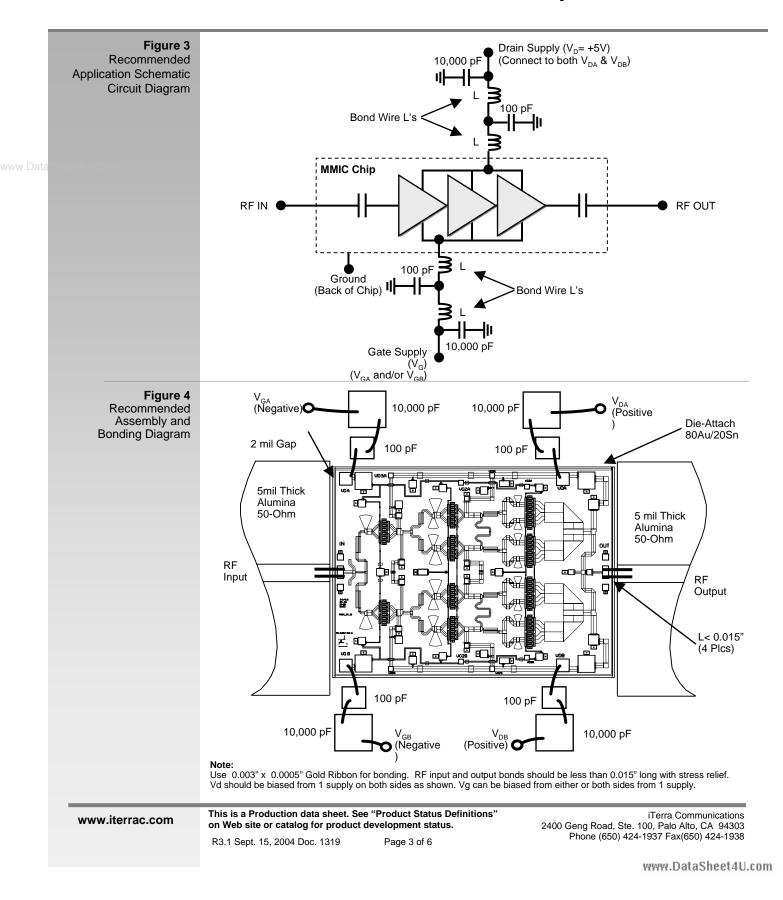
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iTerra Communications 2400 Geng Road, Ste. 100, Palo Alto, CA 94303 Phone (650) 424-1937 Fax(650) 424-1938



Application Information	 CAUTION: THIS IS AN ESD SENSITIVE DEVICE Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes. Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC Ground. These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device. Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 12 mils long corresponding to a typical 2 mil gap between the chip and the substrate material.
Figure 1 Functional Block Diagram	RF IN Ground (Back of Chip) Gate Supply (V _{DA} V _{DB}) (V _D A V _{DB}) (V _D A V _D) (V _D
Figure 2 Chip Layout and Bond Pad Locations (Chip Size=4.282 mm x 3.194 mm x 50 μm. Back of Chip is RF and DC Ground)	Dimensions in mm
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iTR39200 37-40 GHz 1.6 Watt Power Amplifier MMIC



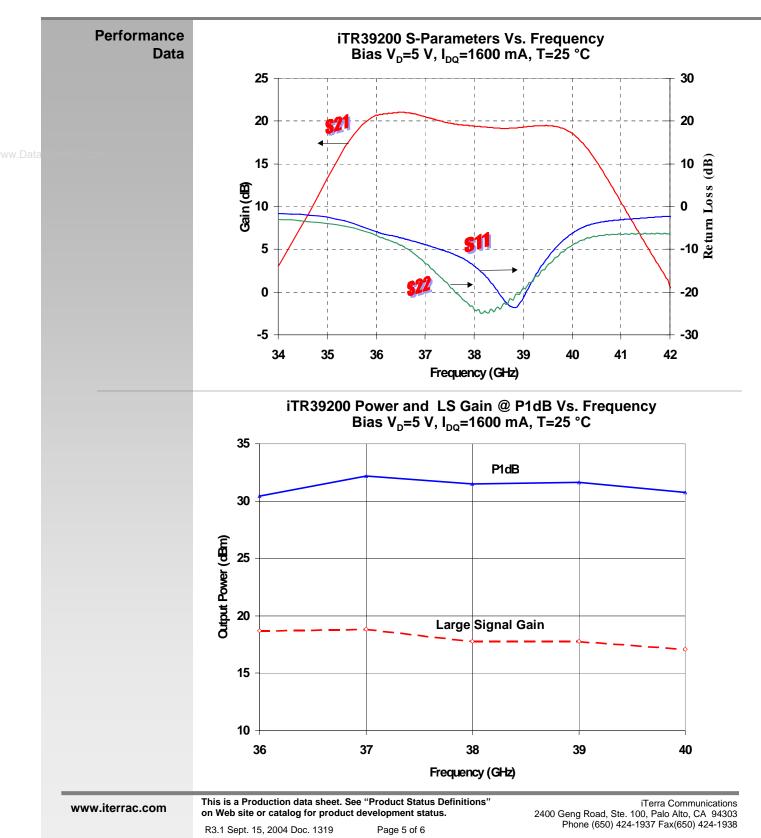


Recommended Procedure for Biasing and Operation	 CAUTION: LOSS OF GATE VOLTAGE (V_G) WHILE DRAIN VOLTAGE (V_D) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP. The following sequence of steps must be followed to properly test the amplifier: Step 1: Turn off RF input power. Step 2: Connect the DC supply grounds to the ground of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5 V to V_G. Step 3: Slowly apply positive drain bias supply voltage of +5 V to V_D. Step 4: Adjust gate bias voltage to set the quiescent current of I_{DQ}=1600 mA. Step 4: Adjust gate bias voltage to set the guiescent current of I_{DQ}=1600 mA.
Application Information Auto-Bias Circuit	Note: An example of an auto bias sequencing circuit to apply negative gate voltage and positive drain voltage for the above procedure is shown below. $+6v \circ \underbrace{D2 D1N6098}_{D1N6098 D3} \underbrace{R1}_{1.0K} \underbrace{C1}_{0.1uF} \underbrace{D1N6098}_{1.0K} \underbrace{C1}_{0.1uF} \underbrace{D1N6098}_{1.0K} \underbrace{C1}_{0.1uF} \underbrace{D1N6098}_{1.0K} \underbrace{C1}_{0.1uF} \underbrace{D1N6098}_{1.0K} \underbrace{C1}_{0.1uF} \underbrace{C1}_{0.1uF} \underbrace{D1N6098}_{1.0K} \underbrace{C1}_{0.1uF} \underbrace{D1N6098}_{1.0K} \underbrace{C1}_{0.1uF} \underbrace{D1N6098}_{1.0K} \underbrace{C1}_{0.1uF} \underbrace{D1N6098}_{1.0K} \underbrace{C1}_{0.1uF} \underbrace{D1N6098}_{1.0K} \underbrace{C2}_{0.47uF} \underbrace{C1}_{0.1uF} \underbrace{D1N6098}_{0.47uF} \underbrace{C1}_{0.1uF} \underbrace{D1N6098}_{0.47uF} \underbrace{D1N6098}_{0.47u$
	$-5v \bigcirc + Adj. For -Vg \\ + Adj. For -Vg \\ + C4 \\ -5v \bigcirc Ori: + 1.80V \\ -5v \bigcirc Ori: + 1.80V \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\$

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